

OUTLINE OF METHOD FOR TRANSPOSING CONTINUOUS LOW FREQUENCY WAVEFORM
(ELECTRO-ENCEPHALOGRAM, ENGINE VIBRATION, ETC) INTO AUDIBLE SOUND FOR
REAL-TIME MONITORING: A SOFTWARE STRATEGY.

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Technologies.

Digitise the raw EEG (line voltage) at the rate of 100 samples per second
(8 bits OK for pilot study, 16 bits would be better).

Assign samples (bytes) sequentially to register of 200 to 400 addresses, ie
2 to 4 seconds of EEG. Call the address of the first sample the right end
of the register, and the address of the last sample the left end, ie the
right is old, the left new.

Read out sequentially from addresses at the rate of 4000 per second (at
this rate, the alpha rhythm, about 7Hz, would be transposed to $40 \times 7 =$
280Hz, about E above middle C.)

The order of reading out of addresses has to reverse repeatedly to stay
within the register. The rules determining when the readout reverses are
the crucial component of the transposition method. For example, the
readout could reverse every time $dV/dT = 0$, ie when a sequence of n
addresses of equal value is read out (value of n to be determined by trial
and error, probably about 3 or 4).

Reversal when $dV/dT = 0$ would ensure that there would be no sudden voltage
reversals causing noisy transients in the output (following D to A
conversion, below). However reversal on every occasion of $dV/dT = 0$ would
be too frequent, causing loss of coherence and high noise levels. Ideally
each reversal should take place at the first and last instances of $dV/dT =$
0 in the register.

Try this: Reserve highest address value (eg 11111111 in 8 bit mode) to be
used as signal to reverse readout order. Place this value in the address
immediately following the last sequence of addresses of equal value (the
right reversal signal), and immediately preceding the first sequence of
addresses of equal value (the left reversal signal). ie addresses have to
be read using a sub-routine to determine the placement of the signals.
(NB the reversal signal must not appear in the output as a high value
address as this would cause a voltage spike in the output. nor should there
be no readout for this address which would cause a negative voltage spike.
One solution is to assign this "pulse" a value equal to the other addresses
of the sequence determining the position of the reversal signal.)

Each time the reversal signal is reached, the register is updated from the
incoming EEG. All values are moved along the register to the right by a
number of addresses equal to the value of t times the sampling rate
(100Hz), where t is the time between the preceding reversal signal and the
current reversal signal. Fill addresses at the left end of the register,
which have been emptied by the shift, with new samples from the EEG.
(NB This step will need to be completed within the interval of one "pulse",
ie a four-thousandth of a second or 250 microseconds. Should be possible at
standard clock-rates? The time available could be increased to say 500 or

750 microseconds by reiterating the value for this address more than once, or using a different software method to trigger reversals. Can give you details if necessary.)

Note that the update will often cause the right reversal signal and preceding address values to "fall off" the right of the register. Therefore provide a buffer region at this end of the register to temporarily accommodate these address values. This is needed only for reversals at the right reversal signal, details below.

To integrate updates and reversals at the left reversal signal proceed as follows: Since the sequence of address values determining the placement of the left reversal signal is shifted along to new addresses, the reversed readout should begin from the new address of the left reversal signal. Simultaneously with the commencement of the reversed readout, revise the position of the right reversal signal (since the previous one may have exited from the right of the register, into the buffer referred to above). Note that the revised position of the right reversal signal must be completed before the readout reaches it.

To integrate updates and reversals at the right reversal signal: begin the reversed readout from the new address of the right reversal signal following the update, as above. Note that this may now occupy the buffer referred to above. Simultaneously with the reversal, revise the position of the left reversal signal (since a new $dV/dT = 0$ may have been entered in the left end of the register by the updates).

Convert the digital output from the readout to analogue for audio monitor, recorder etc.

NB: This method of transposition is perhaps the simplest, but it may cause some degree of undesirable beat modulation. If that is the case we can try a more sophisticated method of reversal which I can describe later. Also this method may not work for stereophonic transposition, since it may be difficult to maintain inter-channel coherence. We can tackle this one later, using methods based on the more sophisticated reversal method. This simple method should at least tell us whether the idea is worth pursuing further.